REMARKS

Claims 1-3 and 6-7 are pending. The Examiner has withdrawn Claims 4-5 from consideration for being directed to non-elected subject matter. By this Amendment, Claims 1-3 and 7 have been amended. No new matter is presented herein.

Allowed Claims

Applicant respectfully acknowledges and appreciates the indication by the Examiner that Claim 6 is allowed.

Allowable Claims

Applicant further respectfully acknowledges and appreciates the indication by the Examiner that Claim 7, although objected to for depending on a rejected base claim, would be in condition for allowance if amended or rewritten to include all of the features of the rejected base claim and any intervening claims.

Claim Rejections - 35 U.S.C. § 103(a)

Claims 1-3 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Hosier (U.S. Patent No. 6,157,019) in view of Perry et al. (U.S. Patent No. 6,548,323, "Perry"). Applicant respectfully traverses the rejection for the following reasons.

Claim 1 recites an image reading device having a plurality of photoelectric conversion elements formed in one or more rows on an IC chip and a metal conductor layer having openings formed therein for limiting light striking the photoelectric conversion elements, wherein the metal conductor layer is formed around the openings

individually so as to prevent light from striking the photoelectric conversion elements except through the openings, and wherein a metal conductor having substantially a same width as the metal conductor layer is formed integrally with the metal conductor layer in an area extending from a photoelectric conversion element located at an end of the row to an edge of the IC chip, and wherein a semiconductor substrate on which the photoelectric conversion elements are formed, the metal conductor layer, and the metal conductor are maintained at a same potential.

Claim 2 recites an image reading device comprising an IC chip, the IC chip comprising: a plurality of photoelectric conversion elements arranged at predetermined intervals in one or more rows on the IC chip and having an opening each; a first metal conductor layer formed around the openings individually to prevent light from striking the photoelectric conversion elements except through the openings; and a second metal conductor layer having substantially a same width as the first metal conductor layer and formed between an edge of the IC chip and the first metal conductor layer in an area extending from a photoelectric conversion element located at an end of the row to the edge of the IC chip so as to shut off light coming obliquely from above in a direction of the edge of the IC chip, and wherein a semiconductor substrate on which the photoelectric conversion elements are formed, the first metal conductor layer, and the second metal conductor layer are maintained at a same potential.

Hosier discloses a plurality of photoelectric conversion elements 12 formed in rows on an IC chip 10 and a metal light shield layer 50 and having openings for limiting light striking the photoelectric conversion elements 12. An opaque filter layer 100 is formed in an area extending from a photoelectric conversion element 12 located at each

end of the IC chip 10 to a chip edge. However, Hosier fails to disclose the opaque filter layer 100 is a metal conductor layer having substantially a same width as a metal light shield layer 50 when the IC chip 10 is seen in plan view.

To address this deficiency in Hosier, the Office Action cites Perry. The Office Action asserts that Perry discloses, in Fig. 2, an opaque material layer deposited on the semiconductor substrate lateral edges. According to Perry, the opaque material can be a variety of metals such as aluminum and titanium, and the thickness of the deposited opaque material layer will depend on the wavelength of light to be blocked. It appears as if the Office Action interprets "the thickness of the opaque meal layer" taught by Perry as "the width of the metal conductor layer" recited by pending Claim 1.

The Applicant respectfully disagrees with the above-mentioned assertions made by the Office Action for the following reasons.

The metal conductor layer recited in Claim 1 is a metal layer serving as a conductor for wiring the photoelectric conversion elements. More specifically, the metal conductor layer is a metal conductor layer connected to one terminal of the photoelectric conversion elements. For example, as evident from Fig. 4B of the instant application, the metal conductor layer 25 is connected to the anodes of photodiodes PD1 – PDn. The present invention also uses the metal conductor layer for preventing light from striking elsewhere other than the openings of the photoelectric conversion elements.

In contrast, the metal light shield layer 50 of Hosier is a metal light shield layer used to shape the openings that permit light to pass therethrough (see column 4, line

47). For this reason, Hosier does not teach or suggest the metal light shield layer 50 is also a conductor for wiring photosites 12.

Regarding Claim 2 of the instant application, the "first metal conductor layer" and the "second metal conductor layer" features recited therein correspond to the above-mentioned "metal conductor layer" so that the above-provided arguments are also applicable with respect to Claim 2, as well.

The metal conductor layer recited in Claim 1 is "formed around the openings" individually to prevent light from striking the photoelectric conversion elements except through the openings. If the openings are rectangular in shape, as shown in an exemplary embodiment of the instant application, all four sides of the rectangular openings are enclosed by the metal conductor layer in plan view. Claim 1 further recites a metal conductor has substantially a same width as the metal conductor layer is formed integrally with the metal conductor layer in an area extending from a photoelectric conversion element located at an end of the row to an edge of the IC chip.

However, the metal light shield layer 50 of Hosier, asserted by the Office Action as corresponding to the metal conductor layer of the present invention, does not correspond to the above-mentioned metal conductor layer 25 of the present invention as explained above. Even if, for argument sake, the metal light shield layer 50 of Hosier corresponds to the metal conductor layer 25 of the present invention, the metal light shield layer 50 of Hosier does not enclose the photosite 12 located at the chip edge. To be more specific, the photosite 12 located at the left side (chip edge portion) in Figs. 7 and 8 are not enclosed by the metal light shield layer 50. The opaque filter layer 100 does not enclose the photosite 12 located at the chip edge.

Regarding Claim 2 of the instant application, the "first metal conductor layer" and the "second metal conductor layer" features recited therein correspond to the above-mentioned "metal conductor layer" so that the above-provided arguments are also applicable with respect to Claim 2 as well.

Claim 1 further recites a semiconductor substrate on which the photoelectric conversion elements are formed, the metal conductor layer, and the metal conductor are maintained at a same potential. Claim 2 further recites a semiconductor substrate on which the photoelectric conversion elements are formed, the first metal conductor layer, and the second metal conductor layer are maintained at a same potential. Regarding these features, the Office Action asserts Hosier shows that the first conductor layer 50 and the opaque layer 100 are connected together by being formed continuously starting from the chip edge. However, for the reasons mentioned above, Applicant respectfully submits that Hosier does not teach or suggest the structural arrangement of the features recited by Claims 1-2. Even if Hosier disclose, for argument sake, such feature, Applicant notes the opaque filter layer 100 of Hosier is a black acrylic filter material or a black polyimide filter material (see column 6 lines 34-46). These materials are commonly known as electrical insulators. This means that Hosier does not disclose the material being a metal. In other words, the technical feature, "a semiconductor substrate on which the photoelectric conversion elements are formed, the metal conductor layer, and the metal conductor are maintained at a same potential" is not taught or suggested by Hosier. Furthermore, Hosier does not teach or suggest this feature at all. In addition, because the layer located at the chip edge in the structure disclosed by Hosier is the opaque filter layer 100 formed of an electrically

insulating material, Hosier does not need to maintain the opaque filter layer 100 and the semiconductor substrate at the same potential so as to prevent an electric short circuit from being established therebetween. A person skilled in the art would not be motivated to modify and/or combine Hosier with teachings from other refrences because of this reason.

In view of the above, Applicant respectfully submits Hosier and Perry, alone or in combination, fail to teach or suggest the invention recited by Claims 1-2. To establish prima facie obviousness, each feature of a rejected claim must be taught or suggested by the applied art of record. See M.P.E.P. 2143.03. Since Hosier or Perry, alone or in combination, do not teach or suggest each and every feature of Claims 1-2, Applicant respectfully submits Claims 1-2 are not rendered obvious by Hosier and Perry, and should be deemed allowable.

Claims 3 and 7 depend from Claim 2. It is respectfully submitted that these dependent claims be deemed allowable for at least the same reason Claim 2 is allowable, as well as for the additional subject matter recited therein.

Applicant respectfully requests withdrawal of the rejection.

Conclusion

In view of the foregoing, reconsideration of the application, withdrawal of the outstanding objection and rejection, allowance of Claims 1-3 and 7, and the prompt issuance of a Notice of Allowability are respectfully solicited.

Should the Examiner believe anything further is desirable in order to place this application in better condition for allowance, the Examiner is requested to contact the undersigned at the telephone number listed below.

In the event this paper is not considered to be timely filed, the Applicants respectfully petition for an appropriate extension of time. Any fees for such an extension, together with any additional fees that may be due with respect to this paper, may be charged to counsel's Deposit Account No. 01-2300, **referencing docket number 103213-00041**.

Respectfully submitted,
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